REMARKS

Applicant has reviewed the Office Action mailed on October 6, 2003, as well as the art cited. Claims 1-66 are pending in this application.

Objection to the Drawings

The Examiner objected to the drawings indicating that they do not show all of the claimed features including a phase detector that is a two-state phase detector that uses XOR logic, a phase detector that is a two-state phase detector that is a sequential phase detector, and a phase detector that is a three-state phase detector as recited in the claims. Applicant respectfully traverses this objection. These elements are shown in element 212 of Figure 2 as described in the specification at p. 6, lines 25-29 and p. 11, lines 3-4. Therefore, withdrawal of the objection is respectfully requested.

Rejections Under 35 U.S.C. § 102

Claims 1-5, 10-14, 19-22, 26-31 and 43-44 were rejected under 35 USC § 102(b) as being anticipated by McCauley, (U.S. Patent No. 4,847,678). Applicant respectfully traverses the rejection.

Claim 1 reads as follows:

> 1. A phase comparator, comprising:
> a phase detector having a first input for receiving a first signal, a second input for receiving a second signal, and an output for providing an error signal indicative of a phase relationship between the first signal and the second signal;
> a digital counter having a first input for receiving the error signal, a second input for receiving a sampling clock signal, and an output for providing a count value; and
> a digital-to-analog converter having an input for receiving the count value and an output for providing an error voltage signal.

In claim 1, the digital counter requires two inputs and an output. This includes the error signal and a sampling clock signal. The term "sampling clock signal" has special meaning in the art. The term "sampling" is defined as:

> A technique in which only some portions of an electrical signal are measured and are used to produce a set of discrete values that is representative of the information contained in the whole.

A sampling clock is used to derive the set of instantaneous values during a sampling process. Thus, in claim 1, the term "sampling clock signal" carries with it the meaning that it is a clock signal that is used to gather a plurality of values during a given sampling period. There is nothing in McCauley that teaches or suggests this limitation of claim 1. For example, McCauley shows in Figures 4A and 4B that the phase error signal (provided to the clock input of counter 52) provides exactly one pulse during the measurement window. Col. 4, lines 29-51 and Col. 5, lines 26-55. This is not a sampling clock as called for in claim 1. Therefore, claim 1 is not anticipated by McCauley.

Claims 2-5 depend from and include the patentable limitations of claim 1 and are thus also allowable.

Claim 10 also include the limitation that the digital counter receives a sampling clock input signal. Therefore, for the reasons identified above with respect to claim 1, claim 10 is also not anticipated by McCauley.

Claims 11-14 and 19-22 depend from claim 10 and are thus also allowable.

Claim 26 reads as follows:

> 26. A method of generating a timing signal, comprising:
> generating an error signal indicative of a phase relationship between a reference clock signal and a feedback signal;
> generating a count value indicative of an amount of phase error during a single event;
> generating an error voltage signal proportional to the count value;
> filtering the error voltage signal to produce a control voltage signal;
> generating the timing signal in response to the control voltage signal; and
> deriving the feedback signal from the timing signal.

In part, claim 26 requires that the error signal generated is "proportional to the count value" and that the count value is "indicative of an amount of phase error during a single event." This is not true with the count in McCauley. In McCauley, each event results in incrementing or decrementing the counter once. Col. 6, lines 10-41. Since the amount by which the counter is incremented is not related to the amount of phase difference, the count value is not "indicative of

an amount of phase error during a single event." Therefore, claim 26 is not anticipated by McCauley.

Claims 27, 29, and 30 depend from claim 26 and are thus also allowable.

Claim 28 depends from claim 27 and is thus also allowable. Further, claim 28 also specifies:

> wherein generating a count value comprises incrementing a digital counter in response to a sampling clock signal during a time when the error signal has a first logic state and wherein generating an error voltage occurs at a time when the error signal transitions from the first logic state to a second logic state

This limitation is missing from McCauley because McCauley does not show a sampling clock and does not show incrementing a counter in response to a sampling clock during the time an error signal has a first logic state. Therefore, claim 28 is not anticipated by McCauley.

Claims 31 and 43 include similar limitations as discussed above with respect to claim 26 and are thus also allowable for the same reasons.

Claim 44 depends from claim 43 and is thus similarly allowable. Further, claim 44 adds a limitation with respect to incrementing and decrementing a counter in response to a sampling clock signal. As discussed above, McCauley does not teach or suggest a sampling clock signal. Therefore, claim 44 is not anticipated by McCauley.

Rejections Under 35 U.S.C. § 103

Claims 6-9, 15-18, 23-24, and 33-41 were rejected under 35 USC § 103(a) as being unpatentable over McCauley, (U.S. Patent No. 4,847,678) and Takeuchi (U.S. Patent No. 5,727,193). Applicant respectfully traverses the rejection.

Claims 6-8 depend from claim 1 and add limitations directed to aspects of the sampling clock signal. The Examiner rejected these claims stating that the limitations of these claims "recite obvious variations of well known timing and synchronization procedures and circuitry and would have been obvious in view of the teachings and suggestions" of the references. The Examiner points to no specific teachings to support this statement. Therefore, Applicant respectfully traverses the statement and requests that the Examiner withdraw the statement or provide a reference and citation to back-up this assertion in the next action. Applicant

respectfully asserts that there is nothing in either reference that teaches or suggests these limitations on the sampling clock signal. As discussed above with respect to claim 1, the primary reference fails to teach or suggest a sampling clock signal. Those arguments are incorporated herein by reference. Applicant respectfully asserts that there is nothing in the secondary reference, alone or in combination with the primary reference, that teaches or suggests the use of a sampling clock signal or the additional limitations found in claims 6-8. Therefore, claims 6-8 are not obvious in light of the art.

Claim 9 also depends from claim 1. Claim 9 adds limitations on the resolution of the counter and the digital to analog converter. The Examiner rejected claim 9 with the same statement used in rejecting claims 6-8. Again, Applicant respectfully asserts that this rejection is not proper as the Examiner has provided no basis for the assertion. Applicant respectfully requests that the rejection be dropped or a reference be provided that demonstrate that these limitations are obvious variations. There is no discussion in either of the references, taken alone or in combination, that addresses the issue of the resolution of these elements. Therefore, claim 9 is also not obvious in light of the references.

Claims 15-17 depend from claim 10 and add similar limitations as claims 6-8 added to claim 1. Therefore, claims 15-17 are also allowable for the reasons identified above with respect to claims 6-8.

Claim 18 depends from claim 10 and adds a similar limitation as claim 9 added to claim 1. Therefore, claim 18 is also allowable for the reasons provided above with respect to claim 9.

Claims 23 and 24 depend from claim independent claim 10 discussed above. There is nothing in the combination of McCauley and Takeuchi that teaches or suggests the limitation missing from claim 10 as discussed above. Therefore, claims 23 and 24 are also not taught or suggested by the references, alone or in combination.

Claims 33 and 40 were rejected for the reasons identified with respect to claims 10, 11, 19, 22, and 23. Applicant respectfully asserts that claims 33 and 40 are allowable based on the arguments above with respect to claims 10, 11, 19, 22, and 23.

Claims 34-39 and 41 were rejected based on the reasons applied to claims 12, 13, 15, 20, 22, and 24. Applicant respectfully asserts that claims 34-39 and 41 are allowable based on the arguments above with respect to claims 12, 13, 15, 20, 22, and 24.

Allowable Subject Matter

Applicant thanks the Examiner for the indication that claims 25, 32, 42, and 45 were allowed over the art of record.

CONCLUSION

Applicant respectfully submits that claims 1-66 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 332-4720.

Respectfully submitted,

Date: January 6, 2004

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